MAS9116

Stereo Digital Volume Control

- **Signal Voltage up to ± 18V**
- **Two Independent Channels**
- **Use of Differential DACs Possible**
- **Serial Control Registers**

DESCRIPTION

MAS9116 is a stereo volume control for audio systems, which require high output voltages (AC3). It has a 16-bit serial interface, which controls two audio channels. Simple serial interface allows microcontroller to control many MAS9116 chips on the same PCB board. “Clicking” between gain changes is eliminated by changing gain only when zero crossing has been detected from the signal. The use of external operational amplifier provides flexibility for the operating voltage, signal swing, noise floor and cost optimization.

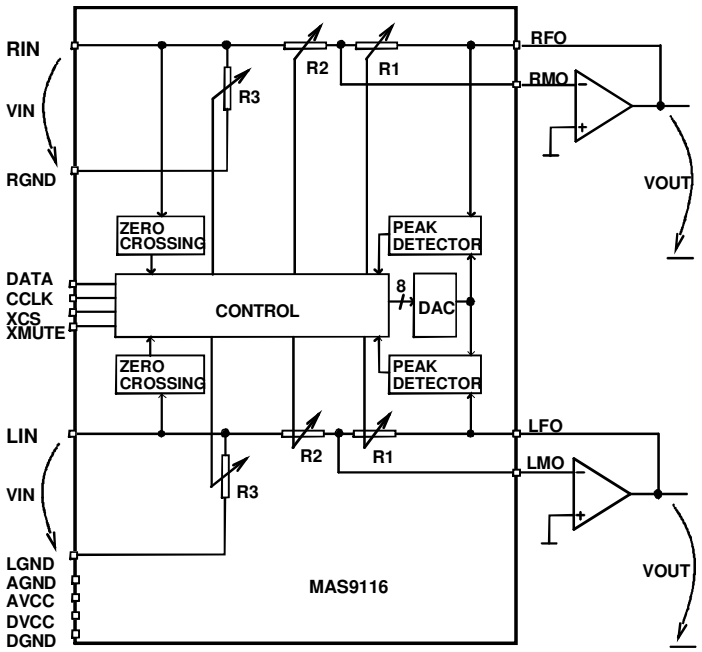
FEATURES

- Zero Detection for Gain Changes
- Gain Range +15.5db…-111.5dB
- 0.5 dB Step Size
- Mute Pin and Register
- Power On/Off Transient Suppression
- Signal Peak Level Comparator with Adjustable Reference

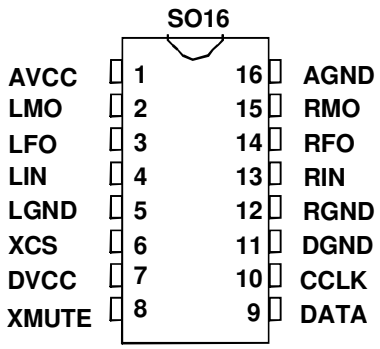
APPLICATION

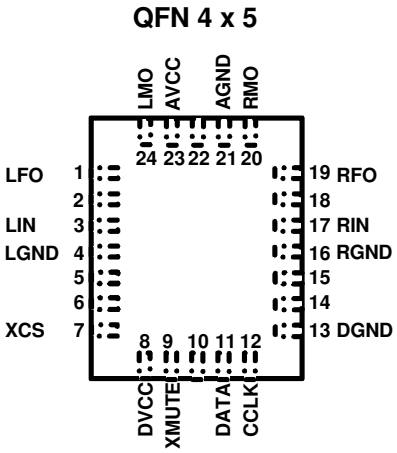
- High End Audio Systems
- Multichannel Audio Systems

BLOCK DIAGRAM



PIN CONFIGURATIONS





PIN DESCRIPTION

Pin Name	Pin SO16	Pin QFN 4x5	Type	Function
AVCC	1	23	P	Power Supply, for Analog
LMO	2	24	AI	External Amplifier Negative Input (Left)
LFO*	3	1	AI	Feedback Signal from External Amplifier Output (Left)
LIN*	4	3	AI	Input, Left Channel
LGND	5	4	AI	Signal Ground, Left Channel
XCS	6	7	DI	Chip Select Input of Serial Interface
DVCC	7	8	P	Power Supply, for Digital
XMUTE	8	9	DI	Mute Input
DATA	9	11	DIO	Data Input and Output of Serial Interface, Tristate
CCLK	10	12	DI	Clock Input of Serial Interface
DGND	11	13	G	Ground for Digital
RGND	12	16	AI	Signal Ground, Right Channel
RIN*	13	17	AI	Input, Right Channel
RFO*	14	19	AI	Feedback Signal from External Amplifier Output (Right)
RMO	15	20	AI	External Amplifier Negative Input (Right)
AGND	16	21	G	Ground for Analog

*) Note: These Pins are only 300V HBM ESD protected

GENERAL DESCRIPTION

Main features

MAS9116 is a stereo digital volume control designed for audio systems. The levels of the left and right analog channels are set by the serial interface. Both channels can be programmed independently. Resistor values are decoded to 0.5 dB resolution by using internal multiplexers for a gain from –111.5 to +15.5 dB. The code for –112 dB activates mute for maximum attenuation. MAS9116 operates from single +5V supply and accepts input levels up to ±18V.

Interfaces

Control information is written into or read back from the internal register via the serial control port. Serial control port consists of a bi-directional pin for data (DATA), chip select pin (XCS) and control clock (CCLK) and supports the serial communication protocol. All control instructions require two bytes of data.

To shift the data in CCLK must be pulsed 16 times when XCS is low. The data is shifted into the serial input register on the rising edges of CCLK pulses. The first 8 bits contain address information. The second byte contains the control word. XCS must return to high after the second byte. That is, after the 16th CCLK XCS must be returned to high. See the timing diagram on page 11.

The same process takes place for reading the information. XCS will remain low for next 16 CCLK pulses. The data is shifted out on the falling edges of CCLK. When XCS is high, the DATA pin is in high impedance state, which enables DATA pins of other devices to be multiplexed together.

On the PCB board the same DATA and CCLK lines can be directed to every MAS9116 chip. If the XCS-pin is not active (low), DATA-pin of that chip is in high-impedance state. This allows using a simple PCB board for multichannel audio systems.

Operating modes

When power is first applied, power-on reset initializes control registers and sets MAS9116 into mute state. The activation of the device requires that XMUTE pin is high and a control byte with a greater than the default value is written in the gain register. It is possible to return to the mute stage either by setting XMUTE pin low or writing zero (00hex) to the gain register.

The device has special test register which is used only for internal testing of the device. It is strongly recommended not to change the initial test register value (00hex) in normal operation. For device testing XMUTE pin is bidirectional. When the test register bit 1 is high, XMUTE pin is output pin. Internal signals can be directed to the pin. Note: In this state the analog output is muted and new gain values cannot be written into the gain register.

Changing the gain of the channel

When new gain value is written into the gain register the chip will activate zero crossing and delay generator for the selected channel. MAS9116 will wait until rising edge zero crossing is detected in the input signal to ensure that there is no audible click from the output of amplifier when gain is changed. LIN is the input line for the left channel and RIN for the right channel. If there are no zero crossings in the signal, the gain is changed after typical 18ms delay, since then the delay generator will provide about 100ns pulse forcing the new value to be latched. The delay generator´s delay has variation but it is guaranteed that the delay is no longer than 50ms.

If new gain value has been written before zero crossing or delay generator´s delay have occured the previous gain value is overwritten, so the previous value is not latched to the output. If it is desired that each gain value will be latched to the output there should be minimum 50ms delay between each gain value writings.

Programming both gain registers at the same time sets gain values first to the right channel and then to the left channel.

Programming gain into left and right channel using separate commands causes gain values to be set in the same order as the programming. If no zero crossings occur in either channel, the firstly written channel´s gain is changed after first channel´s delay generator´s delay has passed. Only after that second channel´s delay generator is started. In these conditions the first channel gain is set after maximum 50ms delay but second channel is set after maximum 50ms+50ms = 100ms delay. To guarantee that each written gain value will be set in all conditions *the maximum programming rate for both channel gains separately is thus 1/100ms = 10 Hz.*

GENERAL DESCRIPTION

Peak Level Detection

MAS9116 has an 8-bit digital-to-analog converter (DAC) used for monitoring the peak level of the signal. The reference value is programmed via the serial interface. The reference value VREF is calculated from VREF=(0.16+0.0133*CODE)*VDD, where CODE is decimal value of the control byte (0..255) and VDD is MAS9116 supply voltage value. With nominal 5 V supply voltage the reference value is VREF=0.8V+66.5mV*CODE. When positive peak signal level at output exceeds this value, comparator signal sets bits 0 and 1 of the status register. The register contents stay high until the peak register has been read.

REGISTER DESCRIPTION

Register	Address Byte								Data Byte	
	7	6	5	4	3	2	1	0	msb…lsb	Function
Peak Detector Status CR4	X	1	0	1	1	R/W	X	X	Output code 00000000 00000001 00000010 00000011	 No overload Right overload Left overload Both overload
Peak Detector Reference CR3	X	1	1	0	0	R/W	X	X	Input code 11111111 11111110 11111101 • • 00000010 00000001 00000000	DAC output VREF(255) VREF(254) VREF(253) • • VREF(2) VREF(1) VREF(0) Note 1
Left Channel Gain CR2	X	1	1	0	1	R/W	X	X	Input code 11111111 11111110 11111101 • • 11100000 00000010 00000001 00000000	Gain dB +15.5 +15.0 +14.5 • • 0.0 -111.0 -111.5 mute
Right Channel Gain CR1	X	1	1	1	0	R/W	X	X	Input code 11111111 11111110 11111101 • • 11100000 00000010 00000001 00000000	Gain dB +15.5 +15.0 +14.5 • • 0.0 -111.0 -111.5 mute
Test, CR5	X	1	1	1	1	R/W	X	X	Reserved	
Both Channel Gains	X	1	0	0	1	W	X	X	Write to both gain registers	

Note 1. Reference voltage is calculated from VREF(CODE)=(0.16+0.0133*CODE)*VDD

Address byte bits:

- Bit 2 is read/write bit (1=read, 0=write).
- X is don't care, recommended high for low power.

Data byte bits:

- All registers get their default value 00Hex except CR3 which gets FFHex during power-on reset.
- Default value for all bits is zero (00hex).

TEST REGISTER CR5 DESCRIPTION

Note: Test register is intended only for internal testing of the device and not supposed to be used in normal operation. It is strongly recommended not to change initial test register value (00hex).

XMUTE pin is output pin when bit 1 is set in register CR5. Bits 2, 3 and 4 select different internal signals. In test phase those signals can be seen via XMUTE pin.

Condition	Data Byte bits								Function
	7	6	5	4	3	2	1	0	
XMUTE=in	0	0	0	0	0	0	0	0	Normal operation
Test, XMUTE=in	0	0	0	0	0	0	0	1	Force latch, note 1
Test, XMUTE=out	0	0	0	0	0	0	1	0	left delay generator
Test, XMUTE=out	0	0	0	0	0	1	1	0	left peak detector
Test, XMUTE=out	0	0	0	0	1	0	1	0	left zero crossing
Test, XMUTE=out	0	0	0	0	1	1	1	0	left enable for zero crossing and delay generator
Test, XMUTE=out	0	0	0	1	0	0	1	0	right delay generator
Test, XMUTE=out	0	0	0	1	0	1	1	0	right peak detector
Test, XMUTE=out	0	0	0	1	1	0	1	0	right zero crossing
Test, XMUTE=out	0	0	0	1	1	1	1	0	right enable for zero crossing and delay generator

Note 1. Forces the new gain value to be latched to resistor network without waiting for zero crossing or delay generator. LSB bit has to be returned to 0 before next gain value can be latched. When force latch is used, both channels are latched with the same value.

ABSOLUTE MAXIMUM RATINGS

All voltages with respect to ground.

Parameter	Symbol	Conditions	Min	Max	Unit
Signal Voltage	RIN, RFO, LIN, LFO		-20	+20	V
Positive Supply Voltage	AVCC, DVCC		-0.5	+6.0	V
All other pins			-0.3	AVCC +0.3	
Storage Temperature	TS		-55	+125	°C
Operating Temperature	TA		-40	+85	°C
ESD (HBM) pins 3, 4, 13 and 14			300		V
ESD (HBM) all other pins			2000		V

Stresses beyond those listed may cause permanent damage to the device. The device may not operate under these conditions, but it will not be destroyed.

RECOMMENDED OPERATION CONDITIONS

(AVCC=+5.0 V, AVSS=0 V, TA=+25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal Voltage	RIN, RFO, LIN, LFO		-18		+18	V
Positive Supply Voltage	AVCC,DVCC		4.5	5	5.5	V
Negative Supply Voltage	AGND,DGND			0		V
Signal Grounds	LGND,RGND			0		V
Operating Temperature	TA		-20	+25	+60	°C

ANALOG CHARACTERISTICS

◆ Analog Inputs/Outputs

(AVCC=+5.0 V, AVSS=0 V, TA=+25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Resistance	RIN	For any gain	7	10	13	kΩ
Input Capacitance	CIN	For any gain		2		pF
Input offset voltage	VIH	External OP277 amplifier, Gain = 15.5 dB Note 1		0.23	1	mV
Supply current Supply current	IVCC IGND	From AVCC From AGND		2.5 2.5	5 5	mA mA
Power supply rejection ratio[1]	PSRR	From AVCC		80		dB

Note 1. Output offset voltage depends on external opamp and selected gain. Low input offset voltage and input bias current opamp is recommended to be used for minimum output offset. OP277 has excellent offset characteristics. Also OP1177 and AD8610 offer good offset performance.

◆ Gain Control

(AVCC=+5.0 V, AVSS=0 V, TA=+25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gain range	G		-111.5		+15.5	dB
Step size	D			0.5		dB
Gain error[1]	DE	Lowest gains guaranteed by design, not tested in production.			0.5	dB
Gain match error[1]	ME	Between channels			0.2	dB
Mute attenuation	MATT		113			dB

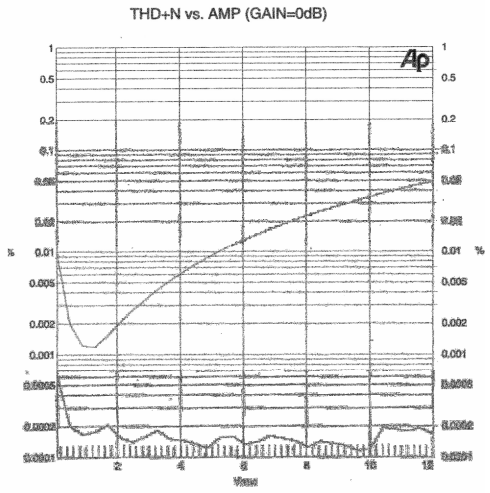
◆ Audio Performance

(AVCC=+5.0 V, AVSS=0 V, TA=+25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Noise[1]	N	Vin=0 Vout with OP275, A-weighting -gain=0dB -gain=-60dB -gain=mute		 4 2.5	13	µVrms
Total harmonic distortion plus noise	THDN	Vin=6Vrms, gain=1, Vout with OP275, 0…20kHz		0.01		%
Dynamic range[1]	DR		120	130		dB
Crosstalk[1]	CR	Between channels, gain=1, fin=1kHz	-100	-110		dB

[1] Guaranteed by design

ANALOG CHARACTERISTICS



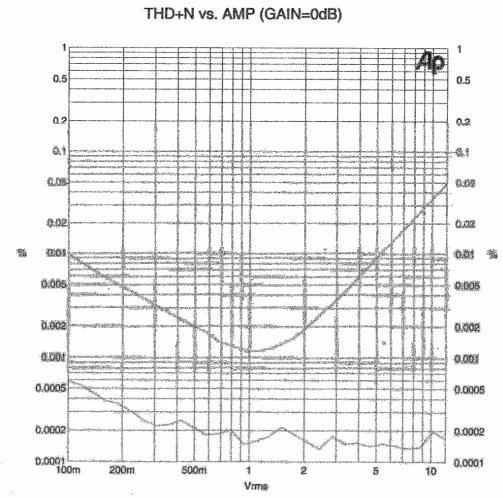


Figure 1 and 2. THD+N vs. input amplitude at 1 kHz, Gain 0 dB. Lower trace is THD+N of Audio Precision Svstem One generator

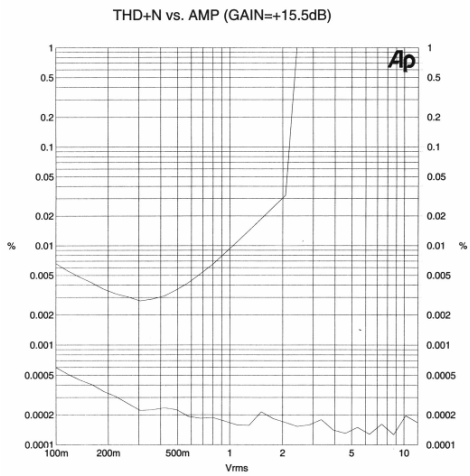


Figure 3. THD+N vs. input amplitude at 1 kHz, Gain +15.5 dB

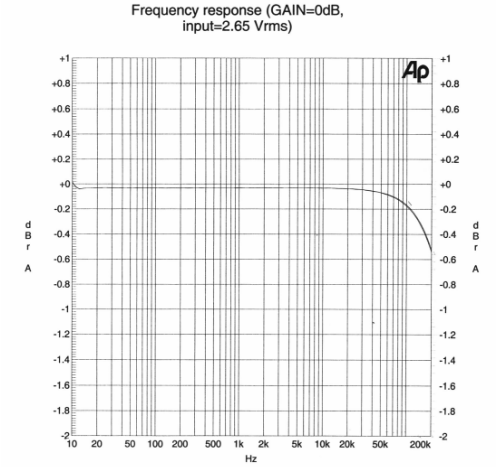


Figure 4. Frequency response, 2.65 Vrms input

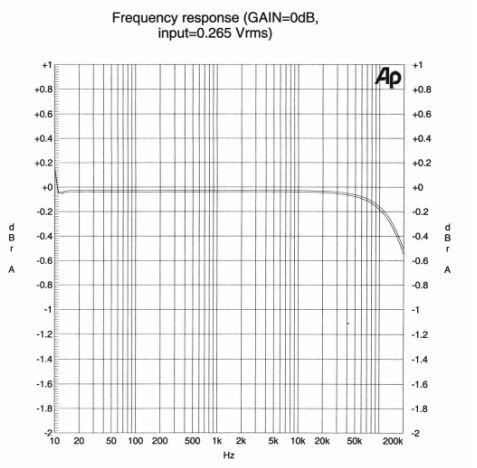


Figure 5. Frequency response, 0.265 Vrms (-20 dB) input

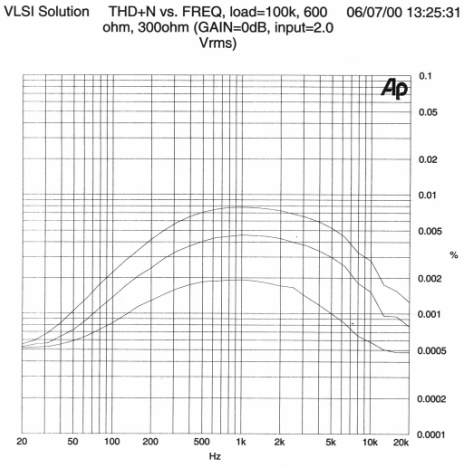


Figure 6. THD+N vs. frequency load = 100kΩ, 600Ω, 300Ω

ANALOG CHARACTERISTICS

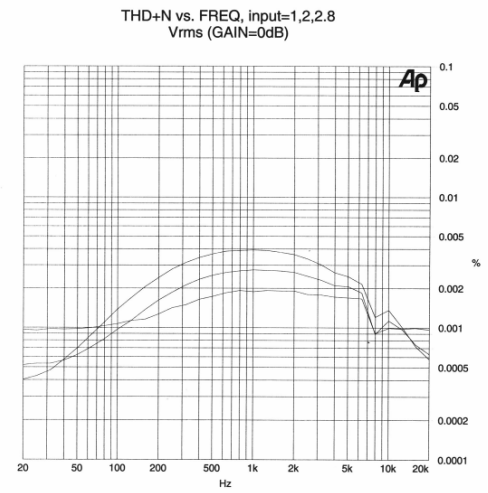


Figure 7. THD+N vs. frequency levels of 1, 2 and 2.8 Vrms

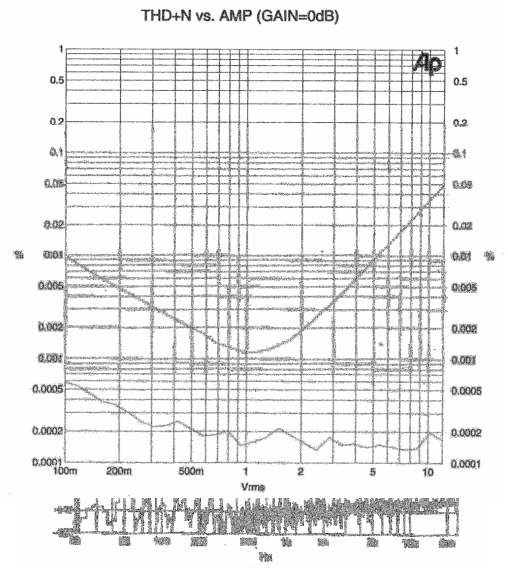


Figure 8. Spectrum, input amplitude 1 Vrms, gain -20 dB

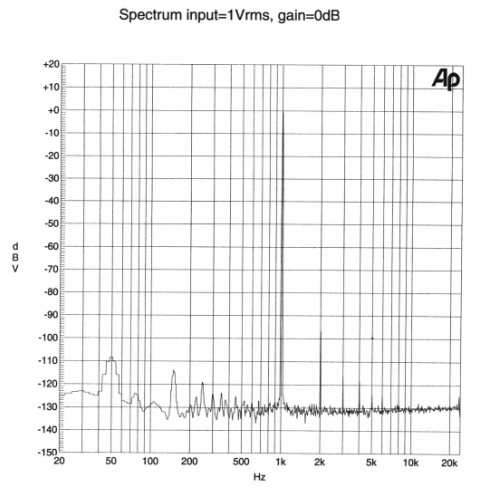


Figure 9. Spectrum, input amplitude 1 Vrms, gain 0 dB

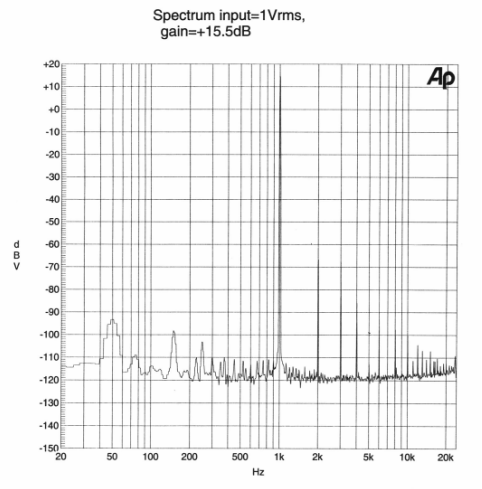


Figure 10. Spectrum, input amplitude 1 Vrms, gain +15.5 dB

DIGITAL CHARACTERISTICS

◆ Digital Inputs/Outputs

(AVCC=+5.0 V, AVSS=0 V, TA=+25°C unless otherwise noted)

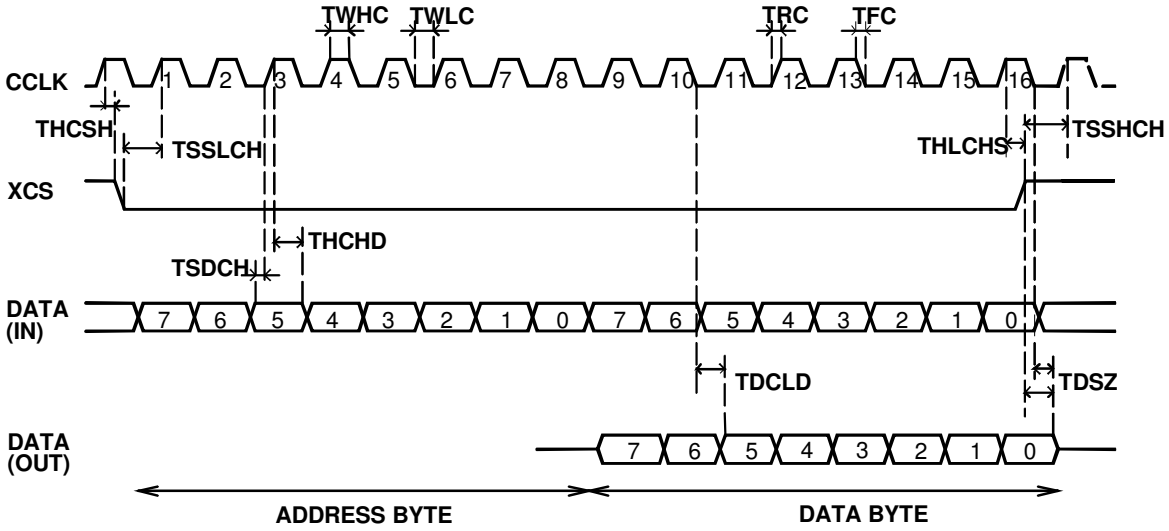
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input low voltage	VIL	All digital inputs, DC			0.3* DVCC	V
Input high voltage	VIH	All digital inputs, DC	0.7* DVCC			V
Output low voltage	VOL	All digital outputs, IL=2mA			0.4	V
Output high voltage	VOH	All digital outputs, IH=2mA	DVCC-0.4			V

◆ Serial Interface Timing

(AVCC=+5.0 V, AVSS=0 V, TA=+25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency of CCLK	FCCLK				1	MHz
Period of CCLK high	TWHC	Measured from VIH to VIH	500			ns
Period of CCLK low	TWLC	Measured from VIL to VIL	500			ns
Rise time of CCLK	TRC	Measured from VIL to VIH			100	ns
Fall time of CCLK	TFC	Measured from VIH to VIL			100	ns
Hold time, CCLK high to XCS low	THCHS		20			ns
Setup time, XCS low to CCLK high	TSSLCH		100			ns
Setup time, valid CI to CCLK high	TSDCH		100			ns
Hold time, CCLK high to invalid CI	THCHD		100			ns
Delay time, CCLK low to valid CI	TDCLD	Load=100pF			200	ns
Delay time, XCS high or 8th CCLK low to invalid CI	TDSZ	Load=3.3kΩ	20		200	ns
Hold time, 16th CCLK high to XCS high	THLCHS		200			ns
Setup time, XCS high to CCLK high	TSSHCH		200			ns

Serial Interface Timing



APPLICATION INFORMATION

Power supply connection and decoupling

To get the best performance of the chip all digital activities should be avoided during analog signal processing.

Important: Analog (AVDD) and digital (DVDD) supply voltage pins should be always connected directly together to keep them in the same voltage potential. No resistor is allowed in connection between AVDD and DVDD (see supply voltage connection circuit in the Application Note 1 on the next page). Otherwise possible voltage difference could trigger latch-up phenomenom which can damage the device. Due to the same reason also the digital control input voltages should not exceed supply and ground voltages as specified in absolute maximum rating specifications on page 6. These requirements are valid also during the startup when supply voltages are applied.

Low noise supply voltages should be used for high quality audio. Supply decoupling capacitors must be located as close to MAS9116 as possible.

Opamp produced output offset voltage

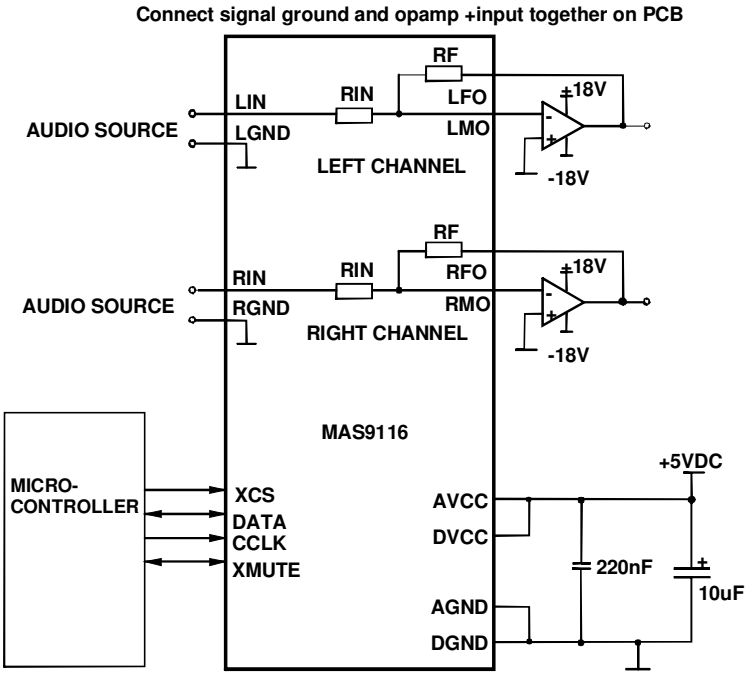
Opamp non-idealities in input offset voltage and in input bias current both produce offset voltage to the output. Since this offset voltage is gain dependent the gain change step can produce dc voltage steps to the output. To achieve the best audio performance it is recommended to use opamps which have both low input offset voltage and low input bias current characteristics. Burr-Brown OP277 has excellent offset and bias and no trimming is needed. Also Analog Devices OP1177 and AD8610 offer very good offset performance. See table below for these and other recommended op-amps.

Manufacturer	Part Number	Typical Output Offset at Maximum Gain (mV)
Analog Devices	OP275	8.5
Analog Devices	OP1177	0.51
Analog Devices	AD8610	1.49
Texas Instruments (BurrBrown)	OP277	0.23
Linear	LT1793	18.5
On-Semi, ST Microelectronics	MC33078	28.4

APPLICATION INFORMATION

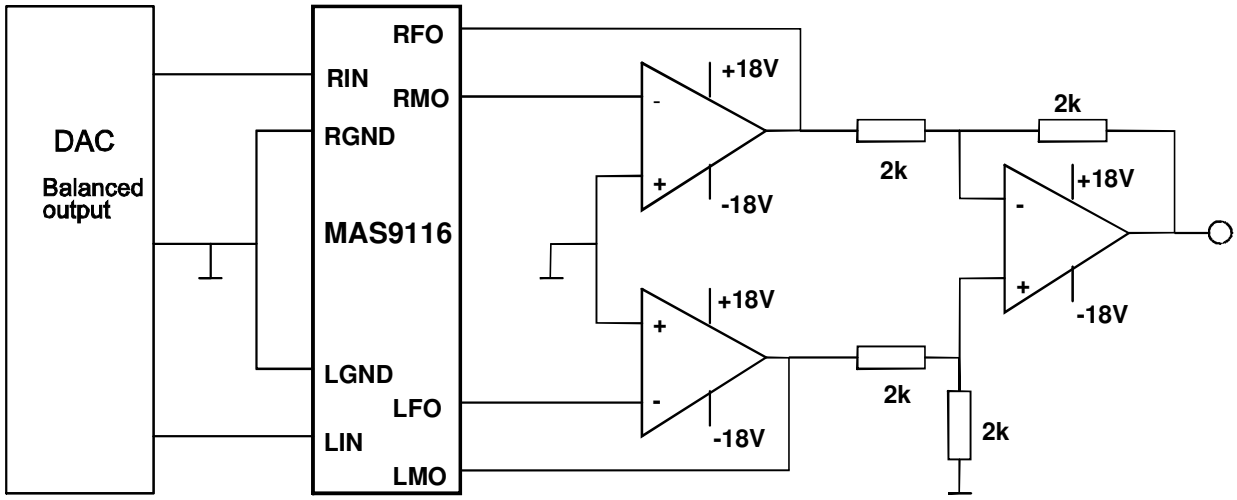
Application Note 1

Typical application



Application note 2

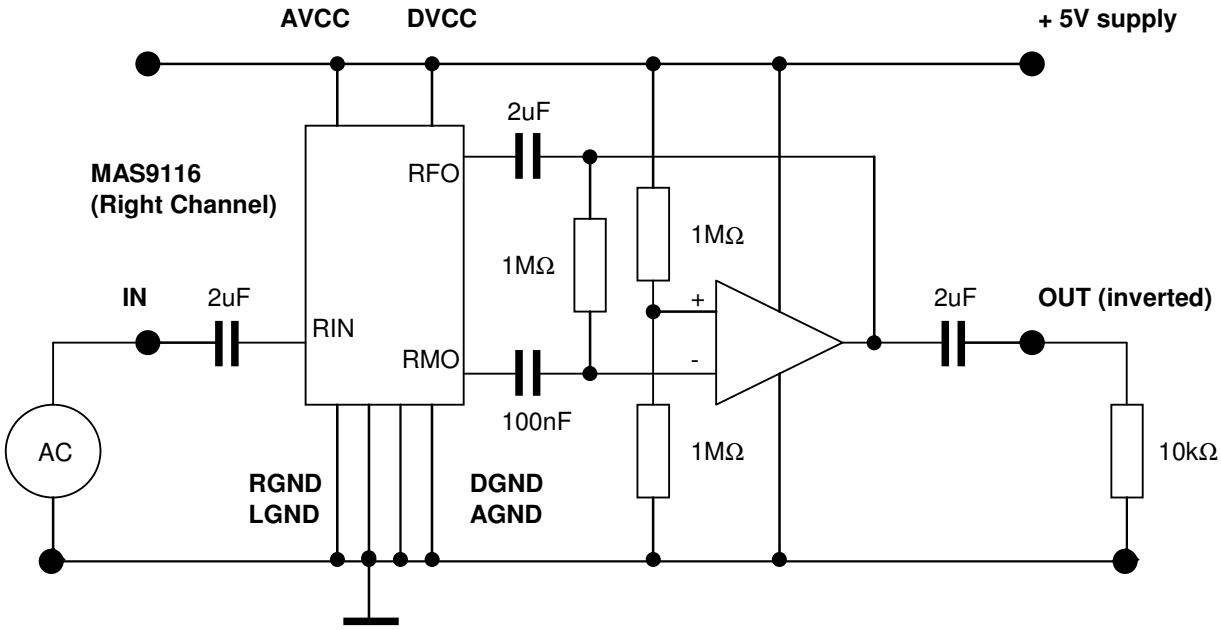
Configuration for balanced output DAC (one channel)



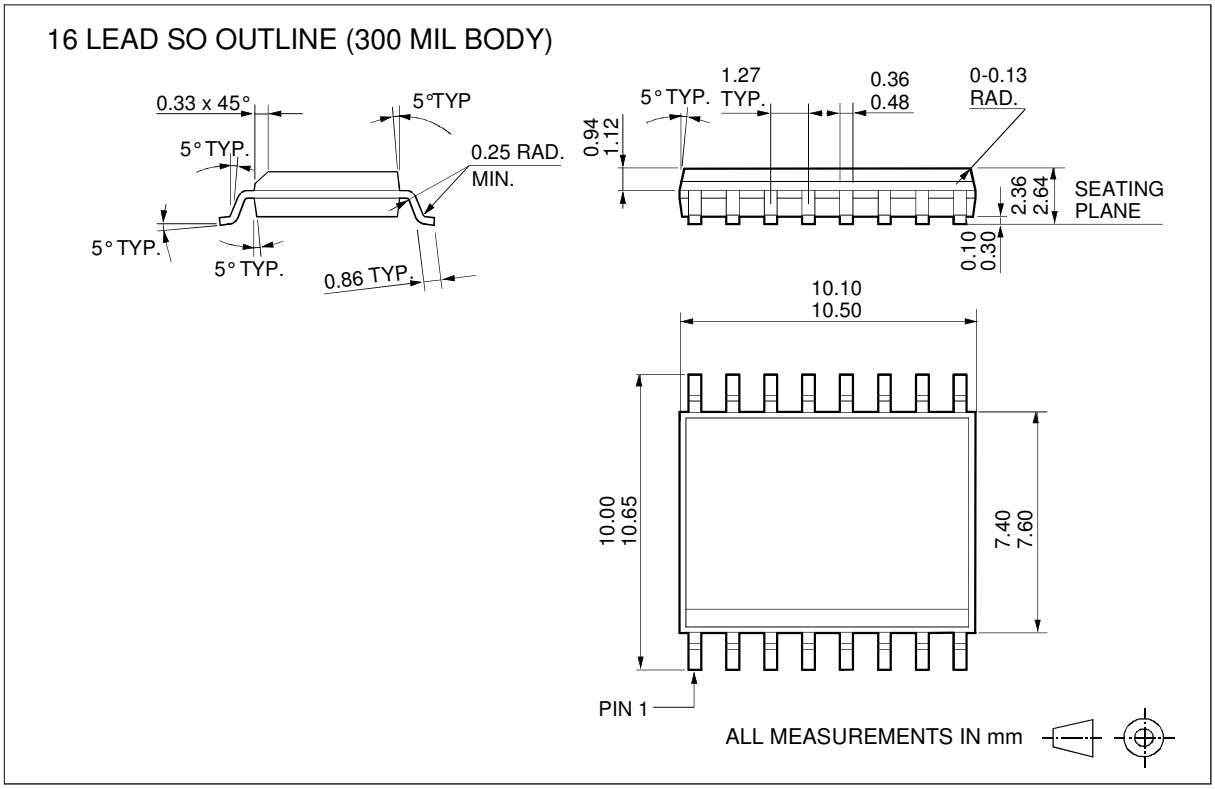
APPLICATION INFORMATION

Application Note 3

Single supply voltage circuit below is based on signal AC coupling and biasing output opamp in the middle point of supply voltages. Note that only right channel circuit is presented. The left channel circuit would be exactly the same. The component values have been chosen to limit lower corner frequency to about 20 Hz.

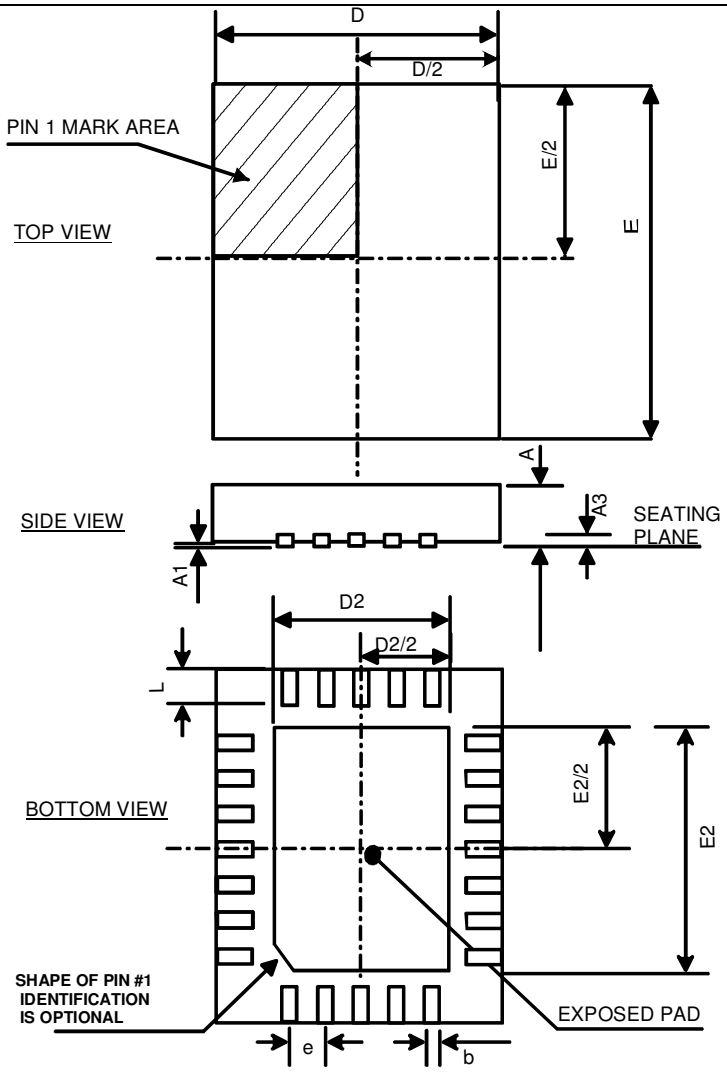


SO-16 PACKAGE OUTLINE



All dimensions are in accordance with JEDEC standard MS-013.

QFN 4x5 24ld PACKAGE OUTLINE



Symbol	Min	Nom	Max	Unit
PACKAGE DIMENSIONS				
A	0.80	0.90	1.0	mm
A1	0	0.02	0.05	mm
A3	0.15	0.20	0.25	mm
b	0.18	0.25	0.30	mm
D		4.00 BSC		mm
D2	2.0	2.15	2.25	mm
E		5.00 BSC		mm
E2	3.0	3.15	3.25	mm
e		0.50 BSC		mm
L	0.45	0.55	0.75	mm

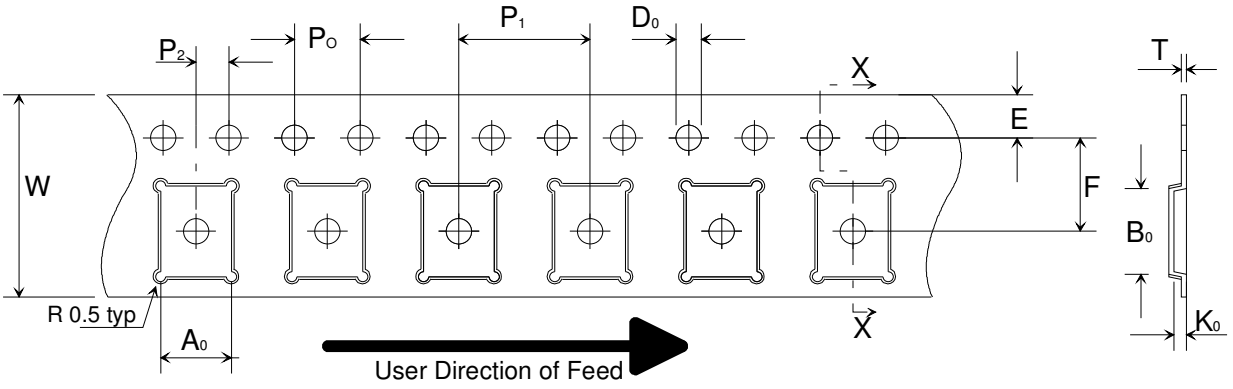
Dimensions do not include mold or interlead flash, protrusions or gate burrs.
All measurements according to JEDEC standard MO-187

SOLDERING INFORMATION

◆ **For Lead-Free / Green QFN 4mm x 5mm**

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

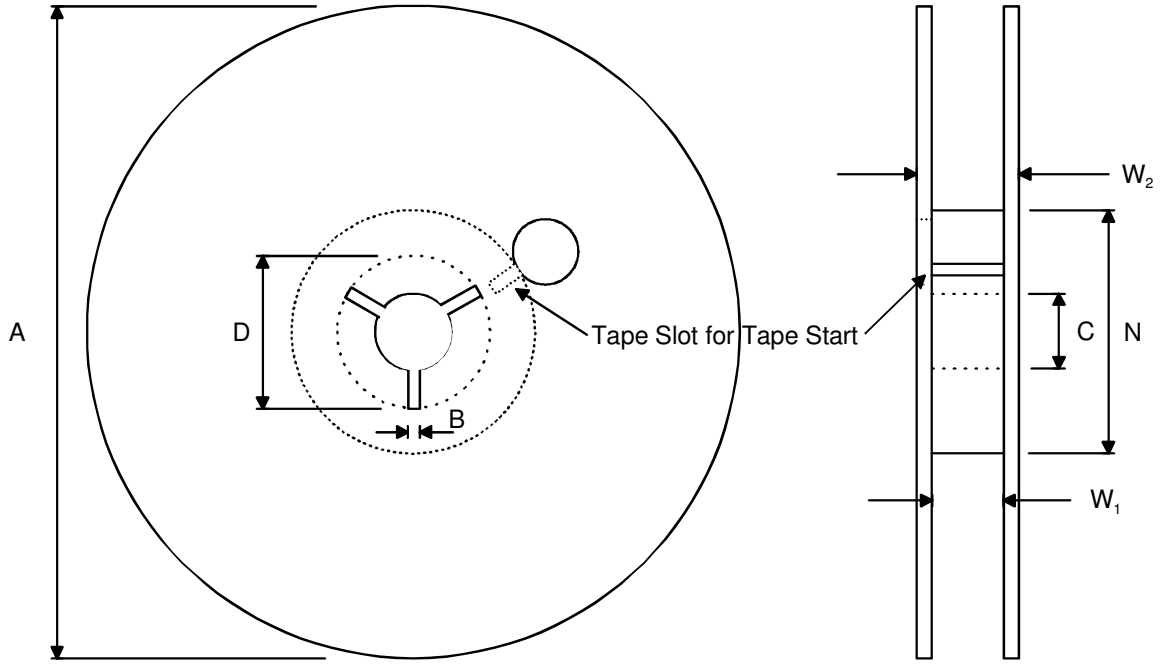
EMBOSSED TAPE SPECIFICATIONS, QFN 4x5 PACKAGE



Dimension	Min/Max	Unit
Ao	4.30 ±0.10	mm
Bo	5.30 ±0.10	mm
Do	1.50 +0.1/-0.0	mm
E	1.75	mm
F	5.50 ±0.5	mm
Ko	1.10 ±0.10	mm
Po	4.0	mm
P1	8.0 ±0.10	mm
P2	2.0 ±0.05	mm
T	0.3 ±0.05	mm
W	12.00 ±0.3	mm

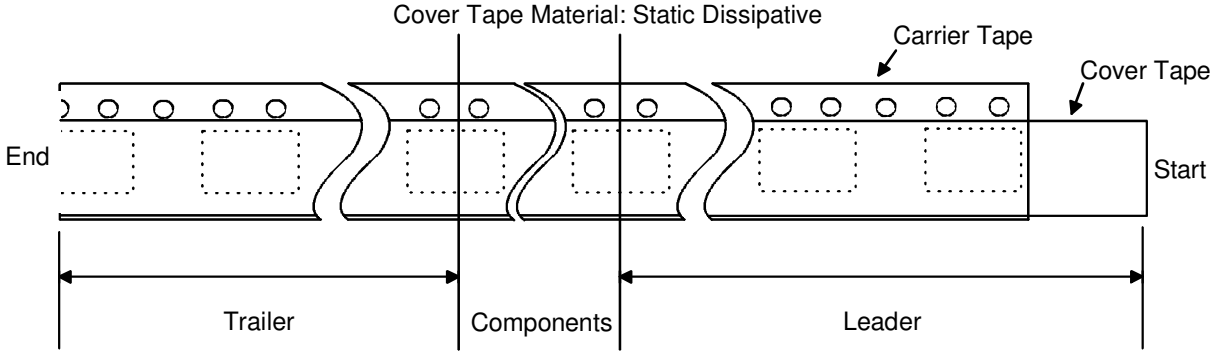
All dimensions in millimeters

REEL SPECIFICATIONS



1000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		178	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W_1 (measured at hub)	8.4	9.9	mm
W_2 (measured at hub)		14.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm

ORDERING INFORMATION

Product Code	Product	Package	Quantity	Comments
MAS9116ASBA-T	MAS9116	16-pin Plastic SOIC	1000 pcs/reel in MBB	MBB=Moisture Barrier Bag
MAS9116ASBA	MAS9116	16-pin Plastic SOIC	47 pcs/tube	MSB0091A Bake recommendation for surface mounted devices
MAS9116AASD06	MAS9116	16-pin Plastic SOIC, RoHS compliant	1000 pcs/reel in MBB	MBB=Moisture Barrier Bag
MAS9116AASD08	MAS9116	16-pin Plastic SOIC, RoHS compliant	47 pcs/tube	MSB0091A Bake recommendation for surface mounted devices
MAS9116AAHV06	MAS9116	24-pin QFN 4x5, RoHS compliant	1000 pcs/reel	MBB=Moisture Barrier Bag

LOCAL DISTRIBUTOR

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